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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,993	10/20/2003	Ok Byung Kim	1514.1031	1374

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EXAMINER	
GUHARAY, KARABI	
ART UNIT	**PAPER NUMBER**
2879	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/687,993	KIM ET AL.	
	Examiner	Art Unit	
	Karabi Guharay	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Response, filed on 27 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,11 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

Response, filed on 27 November 2006 has been considered and entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Recitation of "primary crystal grain boundary" recited in claims 2, and 7-8 renders the claims indefinite since claim 1 recites two sets of primary crystal grain boundaries and their respective inclination, it is not clear which set of primary crystal grain boundaries are referring in this case.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 7-8 & 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitanaga et al. (US 5923997).

Regarding claims 1, 11-12, Mitanaga discloses a display device with a polysilicon substrate (250; Fig 3b and 5a) comprising: a display region (PTFT, 11 l, 133; figure 2; column 13 line 11-column 14 line 55) and a driving region (NTFT; figure 2; column 13 line 11 - column 14 line 55; claims 10-15); a first plurality of thin film transistors in the display region (PTFT; figure 2); a second plurality of thin film transistors (NTFT) and primary crystal grain boundaries (216; figure 5B;column 14 lines 55-65) in the polysilicon substrate in the display region and in the driving region (claim 10), secondary crystal grain boundaries in the polysilicon substrate in the display region and in the driving region (though Mitanaga is silent about secondary crystal grain boundary it is inherent that in crystallization process when crystals are growing, along with the primary grain boundary, secondary grain boundaries are formed perpendicular to the primary grain boundary direction); wherein the primary crystal grain boundaries are inclined to a first direction of current flowing from source to drain of each of the first plurality of TFTs at an angle of -30° to 30° (figure 5b; column 14 line 56 to column 15 line 4; claim 10, the grain boundaries of the first active region are parallel to the direction of current, thereby making that angle 0°); and the secondary crystal grain boundaries are inclined to a second direction of current flowing from source to drain (in this case 90 degrees, since secondary gain boundaries are perpendicular to primary boundaries) of each of the plurality of first plurality of TFts (TFts in the display region) and wherein the primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at an angle of 30°to 150° (claim 10; lines 47- column 16 line 17; claim 10 states that the crystal grain boundaries

in the second region are perpendicular to the current direction, would then be at an angle of 90°), while the secondary crystal grain boundaries are inclined at the first direction of the current flowing from source to drain of each of the second plurality of TFTs (though it is not not disclosed explicitly, it is inherently inclined to 0 degree in this case, since secondary grain boundaries are always perpendicular to the primary grain boundary).

In regard to claim 2, Mitanaga et al ('997) teach the primary crystal grain boundaries (216) are parallel to the first direction of current (column 14 lines 48-55).

In regard to claim 3, Mitanaga et al ('997) teaches a first number of the primary crystal grain boundaries exist in active channel regions of each of the first plurality of thin film transistors (column 13 line 66 to column 14 line 12).

In regard to claim 5, the Applicant is claiming a display device including a method (i.e.: process) of making the polysilicon substrate; consequently, claim 5 is considered a "product-by-process" claim. Inspite of the fact that a product-by-process claim may recite only process limitations, it is the product and not the recited process that is coved by the claim. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. Rather,it is the product itself, which must be new and not obvious (see MPEP 2113). Hence, Mitanaga et al ('997) disclose of a polysilicon substrate meets the structural limitation of the claimed invention.

In regard to claim 7, Mitanaga et al ('997) teach the primary crystal grain boundaries are perpendicular to the second direction of current (column 15 line 48-column 16 line 18).

In regard to claim 8, Mitanaga et al ('997) teach second number of the primary crystal grain boundaries exist in active channel regions of each of the second plurality of thin film transistors (column 15 line 48-column 16 line 18).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7, 8,11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitanaga et al. (US 5923997), and further in view of Iwasaki (US 5759879).

In regard to claims 1 and 12, Mitanaga et al ('997) teach a display device with a polysilicon substrate (250; figures 3b and 5a; column 13 line 47 to column 14 line 55), comprising: a display region (PTFT, 11 l, 133; figure 2; column 13 line 11-column 14 line 55) and a driving region (NTFT; figure 2; column 13 line 11 - column 14 line 55; claims 10-15); a first plurality of thin film transistors in the display region (PTFT; figure 2); a second plurality of thin film transistors (NTFT) and primary crystal grain boundaries

(216; figure 5B;column 14 lines 55-65) in the polysilicon substrate in the display region and in the driving region (claim 10), secondary crystal grain boundaries in the polysilicon substrate in the display region and the driving region (claim 10 states that both active regions have at least one grain boundary, claims 13 and 14 teach that the TFTs are used for both a display region and a driver region); wherein the primary crystal grain boundaries are inclined to a first direction of current flowing from source (208) to drain (210) of each of the first plurality of thin film transistors at an angle of-30° to 30° (figure 5b; column 14 line 56 to column 15 line 4; claim 10, the grain boundaries of the first active region are parallel to the direction of current, thereby making that angle 0°); and wherein the primary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the second plurality of thin film transistors at an angle of 30° to 150° (claim 10; lines 47- column 16 line 17; claim 10 states that the crystal grain boundaries in the second region are perpendicular to the second current in the second TFT - the first current being in the first TFT – these primary crystal grain boundaries in the second region being perpendicular to the current would then be at an angle of 90°). Mitanaga et al ('997) are silent regarding the limitations of the secondary crystal grain boundaries are inclined to a second direction of current flowing from source to drain of each of the first plurality of thin film transistors, and the secondary crystal grain boundaries are inclined to the first direction of the current flowing from source to drain of each of the second plurality of thin film transistors.

In the same field of endeavor, Iwasaki ('879) teaches a display device with comprising well known crystal grain bundies of TFTs (figure 7a) having primary grain boundary and

secondary grain boundary which is perpendicular to the primary grain boundary. Thus, Iwaskai teaches that it is known in the art to grow secondary crystal grain boundaries inclined to a second direction of current flowing from source to drain of each of a first plurality of thin film transistors, and the secondary crystal grain boundaries are inclined to the first direction of the current flowing from source to drain of each of the second plurality of thin film transistors (figures 7a and 7b, column 1 lines 49 to 55).
Thus one skilled in the art would reasonably contemplate that the secondary grain boundary with a fixed relation with the primary grain boundaries of Iwasaki would be an obvious matter of design engineering in the device of Mitanaga et al ('997), as evidenced by Iwasaki ('879). Applicant's claimed material does not provide unexpected results that are not within the teaching applied, since both the grain boundary configurations in Mitanaga and Iwasaki as well as the grain boundaries disclose by the Applicant perform the same function of controlling the carrier mobility of the TFT's (Iwasaki column 1 lines 29-40). Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to incorporate the grain boundary configurations of Iwasaki with the TFT in the display device as taught by Mitanaga et al. Motivation to combine would be to control the carrier mobility of the TFT's within a display device. Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to incorporate the grain boundary configurations of Iwasaki with the TFT in the display device as taught by Mitanaga et al. Motivation to combine would be to control the carrier mobility of the TFT's within a display device.

In regard to claim 2, Mitanaga et al ('997) teach the primary crystal grain boundaries (216) are parallel to the first direction of current (column 14 lines 48-55).

In regard to claim 3, Mitanaga et al ('997) teaches a first number of the primary crystal grain boundaries exist in active channel regions of each of the first plurality of thin film transistors (column 13 line 66 to column 14 line 12).

In regard to claim 4, Mitanaga/Iwasaki disclose all the limitations set forth, as described above, except the display device is an OLED. The Applicant, however, states that using TFTs in organic electroluminescent displays is known in the art in paragraph 9. The MPEP states that "[w]here the specification identifies work done by another as "prior art," the subject matter so identified is treated as admitted prior art. In re Nomiya, 509 F.2d 566, 571,184 USPQ 607, 611 (CCPA 1975). Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to use the polysilicon substrate of Mitanaga/Iwasaki as an OLED substrate. Motivation for combining would be to fabricate an active matrix display.

In regard to claim 5, the Applicant is claiming a display device including a method (i.e.: process) of making the polysilicon substrate; consequently, claim 5 is considered a "product-by-process" claim. In spite of the fact that a product-by-process claim may recite only process limitations, it is the product and not the recited process that is coved by the claim. Further, patentability of a claim to a product does not rest merely on the difference in the method by which the product is made. Rather, it is the product itself, which must be new and not obvious (see MPEP 2113). Hence, Mitanaga et al ('997)

disclose of a polysilicon substrate meets the structural limitation of the claimed invention.

In regard to claim 7, Mitanaga et al ('997) teach the primary crystal grain boundaries are perpendicular to the second direction of current (column 15 line 48-column 16 line 18).

In regard to claim 8, Mitanaga et al ('997) teach second number of the primary crystal grain boundaries exist in active channel regions of each of the second plurality of thin film transistors (column 15 line 48-column 16 line 18).

In regard to claim 11, Mitanaga et al ('997) teach a display device with a polysilicon substrate comprising: a driving region (claim 13); a plurality of thin film transistors in the driving region (claim10); and primary crystal grain boundaries in the polysilicon substrate in the driving region (claim 10); and secondary primary crystal grain boundaries in the polysilicon substrate in the driving region (claim10). Mitanaga et al are silent regarding the limitations of wherein the primary crystal grain boundaries are inclined to a direction of current flowing from source to drain of each of the plurality of thin film transistors at an angle of 30° to 150° and the secondary crystal grain boundaries are substantially parallel to the current flowing from the source to the drain.

In the same field of endeavor, Iwasaki ('879) teaches a display device comprising a polysilicon substrate showing well known primary as well as secondary crystal grain boundaries of active region of theTFTs (figure 7a). Iwaskai teaches it is known in the field to grow primary crystal grain boundaries inclined to a direction of current flowing from source to drain of each of the plurality of thin film transistors at an

angle of 30° to 150° and the secondary crystal grain boundaries grown substantially parallel to the current flowing from the source to the drain (figures 7a and 7b; column 1 lines 49 to 55; teach that there are two different sets of grain boundaries). One skilled in the art would reasonably contemplate incorporating the grain boundaries of Iwasaki in the device of Mitanaga et al ('997), as an obvious matter of design engineering as evidenced by Iwasaki ('879). Applicant's claimed material does not provide unexpected results that are not within the teaching applied, since both the grain boundary configurations in Mitanaga and Iwasaki as well as the grain boundaries disclose by the Applicant perform the same function of controlling the carrier mobility of the TFTs (Iwasaki column 1 lines 29-40). Thus, it would have been obvious at the time of the invention to one of ordinary skill in the art to incorporate the grain boundary configurations of Iwasaki with the TFT in the display device as taught by Mitanaga et al. Motivation to combine would be to control the carrier mobility of the TFT's within a display device.

Response to Arguments

Applicant's arguments filed 27 November have been fully considered but they are not persuasive.

Applicant's argument is concerned about Iwasaki discloses a method of forming a TFT and teaches that the number of grain boundaries is reduced and the position of the grain boundaries are controlled. Examiner agrees, but that does not conclude that Iwasaki shows primary and secondary grain boundaries and their relative inclination with the direction of current. Examiner intends to show through Iwasaki reference that it

is well known while in the process of crystallization, crystal grain boundaries are generally divided into primary grain boundary, which is perpendicular to the growth of the crystal, and secondary crystal grain boundary is formed in the same direction as the crystal growing direction.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is 571-272-2452. The examiner can normally be reached on Monday-Friday 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on 571-272-2457. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K Guharay

Karabi Guharay
Primary Examiner
Art Unit 2879
2/15/07